# LOW VOLTAGE NON-VOLATILE MEMORY CELL

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## FIELD OF THE INVENTION

**[0001]** The present invention relates to a structure for measuring mask and layer alignment in semiconductor fabrication processes.

## RELATED ART

**[0002]** A non-volatile memory cell is a memory cell that retains its stored information even if power is removed from the cell. In a conventional nonvolatile memory cell, a floating gate structure is commonly incorporated to provide this information storage function. Fig. 1 shows an example of a conventional floating gate memory cell 100. Memory cell 100 comprises a polysilicon floating gate 121 surrounded by an insulation material (e.g. silicon dioxide) 150. Floating gate 121 is located over a portion (channel) of a p-type body region 113 extending between an n-type source region 111 and an n-type drain region 112, all of which are formed in a substrate (e.g. silicon wafer) 101. A control gate 120 is located on the portion of insulation material 150 over floating gate 121. Source region 111, drain region 112, and control gate 120 are coupled to receive a source voltage Vs, a drain voltage Vd, and a gate voltage Vg, respectively.

**[0003]** Current between source region 111 and drain region 112 is controlled by the programmed/erased state of floating gate 121. This programmed/erased state is determined by the number of electrons stored (captured) in floating gate 121. In an unprogrammed state, a gate voltage Vg applied to control gate 120 controls the current flow between source region 111 and drain region 112 (i.e. memory cell 100 conducts when voltage Vg is HIGH, and does not conduct when voltage Vg is LOW). To program memory cell 100, electrons are injected into floating gate 121 until it stores a net negative charge that is sufficient to shift the threshold voltage of memory cell 100. Once programmed, memory cell 100